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Attention: Mr. Michael Hall

Dear Sirs

TINGGI TECHNOLOGIES PTE LTD
PCT INTERNATIONAL PATENT APPLICATION NO. PCT/SG2003/00223
"FABRICATION OF SEMICONDUCTOR DEVICES"

We refer to your Written Opinion dated 27 May 2005.

We enclose re-typed amended claims on replacement pages 14 to 17 and, for the examiner's convenience, manuscript amended pages.

The effect of the amendment is to clarify that the relatively thick layer of the thermally conductive metal on the first ohmic contact layer is to form a heat sink, and to incorporate the subject matter of old claim 30 into claim 29. The remaining claims have been re-numbered.

The examiner has found old claim 30 to be novel over D1. Therefore, we submit that new claim 29 and dependent claims 30 to 36 are also novel over D1.

The examiner considers old claims 29-42 to be obvious over D1. Firstly, we submit that there is nothing in D1 to suggest that the support layer 1119 acts as a heat sink. Column 7 line 35 simply suggests that the support layer is structurally strong enough to withstand handling and thin enough to allow the semiconductor membrane to be cleaved. Further, we wish to point out to the examiner that at support layer is deposited by electroplating onto exposed semiconductor membrane (column 7 line 30). This differs from the present invention where the relatively thick layer of thermally conductive metal is electroplated on the first ohmic contact layer.

Secondly, there is nothing in D1 to suggest an adhesive layer. In fact, D1 teaches away from an adhesive layer by requiring the step of removing the bonding material so that the semiconductor device can be transferred from the support substrate onto final substrate. There is no "final substrate" in the present invention as claimed.

Therefore, in light of the above, we submit that the newly amended claims are novel and inventive over the cited document.

The following sections relate to the corresponding sections in Box VIII of the Written Opinion.

1. The examiner considers the claims as a whole are not clear and do not relate to a single invention. The search examiner was able to carry out a meaningful search of the technical features of the claims and did not raise any clarity nor lack of unity objections. Therefore, we submit that the claims are clear and the objection should be withdrawn.

2. The examiner is correct to have taken "wafer" and "substrate" to be the same as they refer to the layer on which the semiconductor devices of the claims are formed. It is known by a person skilled in the semiconductor industry that a substrate is a wafer of material, normally a single crystal, upon which semiconductor devices can be fabricated using epitaxial crystal growth and photolithography.

3. The examiner considers that the term "relatively" in claims 1 and 29 is not clear. We submit that the term "relatively" refers to the layer being relatively thick as opposed to relative to a particular feature. We draw the examiner's attention to page 6 line 10 of the description where it explains that the relatively thick layer may be at least 50 micrometers thick. Therefore, we submit that the objection should be withdrawn.

4. The examiner considers that claims 38 and 43 are not supported by the description. The applicant respectfully disagrees and directs the examiner to page 6, lines 23-26 and page 7, lines 3-9. Further, the semiconductor device in claim 38 includes a thermally conductive metal on the adhesive layer. Although it is correct (as usual) that the claims are broader in scope than the embodiments described, we submit that a person skilled in the art would readily be able to extend the teachings of the description across the whole scope of the claim. Therefore, we submit that the objection should be withdrawn.

5. The examiner considers claim 38 is not clear with respect to the function of the seed layer. We draw the examiner's attention to page 8, lines 20-25 and page 9, lines 21-24 where it states that a copper seed layer of thermally conductive metal such as copper is added to the ohmic contact layer. It goes on to state that this thermally conductive metal is preferably also electrically conductive. Therefore, we submit that the claim is clear and the objection should be withdrawn.

We look forward to a clear report.

Yours faithfully,

Keith Callinan
Patent Attorney
ALBAN TAY MAHTANI & DE SILVA

Encl.

21. A method as claimed in any one of claims 15 to 20, wherein after forming the second ohmic contact layer there is included testing of the semiconductor devices on the wafer.

22. A method as claimed in any one of claims 15 to 21, wherein there is included the step of separating the wafer into individual devices.

23. A method as claimed in any one of claims 1 to 22, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

24. A method as claimed in any one of claims 1 to 23, wherein the wafer includes epitaxial layers and, on a first surface of the epitaxial layers remote from the substrate, a first ohmic contact layer; the first ohmic contact layers being on p-type layers of the epitaxial layers.

25. A method as claimed in any claim 22, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

26. A method as claimed in any one of claims 1 to 14, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer and bond pads deposited on the epitaxial layers.

27. A method as claimed in any one of claims 1 to 14, wherein after step (c), electroplating of a thermally conductive metal on the epitaxial layers is performed.

28. A method as claimed in any one of claims 24 to 27, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

29. A semiconductor device comprising epitaxial layers, first ohmic contact layers on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer to form a heat sink, and a second ohmic contact layer on a second surface of the epitaxial

layers an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer; the relatively thick layer being applied by electroplating.

~~30.A semiconductor device as claimed in claim 29, wherein there is an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.~~

~~31.~~30. A semiconductor device as claimed in claim ~~30~~29, wherein there is a seed layer of the thermally conductive metal, applied to the adhesive layer.

~~32.~~31. A semiconductor device as claimed in any one of claims 29 ~~to 31~~and 30, wherein the relatively thick layer is at least 50 micrometers thick.

~~33.~~32. A semiconductor device as claimed in any one of claims 29 to ~~32~~31, wherein the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

~~34.~~33. A semiconductor device as claimed in any one of claims 29 to ~~33~~32, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

~~35.~~34. A semiconductor device as claimed in any one of claims 29 to ~~34~~33, wherein the second ohmic layer includes bonding pads.

~~36.~~35. A semiconductor device as claimed in any one of claims 29 to ~~35~~34, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

~~37.~~36. A semiconductor device as claimed in any one of claims 29 to ~~36~~35, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

~~38.~~37. A semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

39.38. A semiconductor device as claimed in claim 3837, further including a relatively thick layer of the thermally conductive metal on the seed layer, the relatively thick layer acting as a heat sink.

40.39. A semiconductor device as claimed in claim 38-37 or claim 3938, further including a second ohmic contact layer on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

41.40. A semiconductor device as claimed in any one of claims 38-37 to 4039, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of : opaque, transparent, and semi-transparent.

42.41. A semiconductor device as claimed in any one of claims 38-37 to 4140, wherein the thermally conductive metal comprises copper; and the epitaxial layers comprise GaN-related layers.

43.42. A method of fabrication of a semiconductor device, the method including the steps:

(a) on a substrate with a wafer comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the wafer;

(b) removing the substrate from the wafer; and

(c) forming a second ohmic contact layer on a second surface of the wafer, the second ohmic contact layer having bonding pads formed thereon.

44.43. A method as claimed in claim 4342, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

45.44. A method as claimed in claim 43-42 or claim 4443, wherein the second ohmic contact layer is one of: blank, and patterned.

46.45. A semiconductor device fabricated by the method of any one of claims 43 42 to 4544.

47.46. A semiconductor device as claimed in claim 4645, wherein the semiconductor device is one of: a light emitting device, and a transistor device.

48.47. A method for fabrication of a semiconductor device on a substrate, the semiconductor device having wafer with a device layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the device layer; and

(b) removing the substrate.

49.48. A method as claimed in claim 4847, wherein the semiconductor device is a silicon-based device.

50.49. A method for fabrication of a light emitting device on a substrate, the light emitting device having wafer with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the wafer remote from the substrate and close to the active layer; and

(b) removing the substrate.

51.50. A method as claimed in any one of claims 48 47 to 5049, wherein the thermally conductive layer is as a heat sink.

52.51. A method as claimed in claim 5150, wherein the thermally conductive layer is of a thickness in the range of from 3 microns to 300 microns.

53.52. A method as claimed in claim 51 50 or claim 5251, wherein the thermally conductive layer is of a thickness of from 50 to 200 microns.